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" ENERGY – EFFICIENT DESIGN AND SIMULATION OF A MIMO-OFDM DECODER FOR LOW POWER WIRELESS APPLICATIONS"

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ABSTRACT

In this paper, we present the design and modelling of the Viterbi Decoder for a wireless communication system with multiple inputs and multiple outputs. To verify the receipt of accurate data, it is crucial to detect the mistakes that are introduced into wireless environment signals. Due to advancements in wireless communication technologies, transmitters and receivers are continually exchanging vast amounts of data. Numerous additional communication signals, noise generated randomly by machines, noise produced by people, and noise produced by nature all interfere with this data. Therefore, the receiver needs a good mechanism to generate the original communicated data. Such a system guarantees accurate data processing and prevents the creation of any undesirable output. In the current work, a single bit mistake that occurred during the transmission of an encoded data symbol is successfully corrected by designing an error detection and repair Viterbi decoding method. Xilinx software is used to verify the simulation.

Key Words: *Burst Error, Convolutional Code , Error correction code, Error detection code, FPGA, Interleaver, Convolutional Viterbi Decoder, Xilinx ISE.*

I. INTRODUCTION

The current communication process modifies the communication signal in the wireless environment due to the growing signal congestion. The data processing systems need a highly powerful channel noise rejection component to make the communication successful. There are several ways to either lessen the impact of faults or to find and fix them. Multiple antennas are used to transmit data in a Multiple-Input-Multiple-Output (MIMO) system. The performance of the communication system is improved by the MIMO implementation. Additionally, it results in a higher utilization of channel bandwidth. An improvement in communication data throughput is also brought about by parallel data transfer. Utilizing multiple antennas has the consequence of introducing many signals into the environment, making noise and other interference signals more severe as they may influence parallel data.

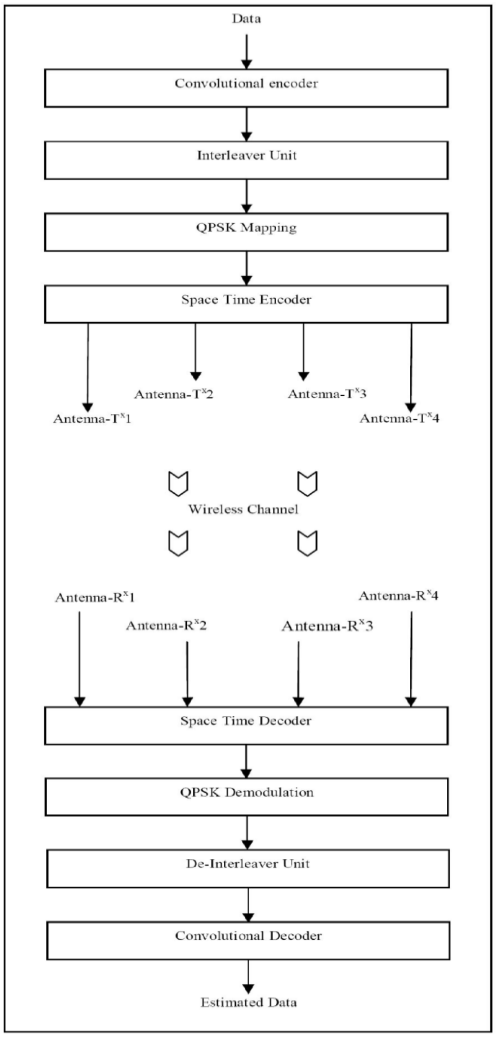
Most LAN-based systems choose to employ the Orthogonal Frequency Division Multiplexing (OFDM) technology for transferring the data symbols in wireless systems involving high data rate connection. In MIMO systems, this strategy is more efficient. A crucial feature of large capacity data systems is the veracity of the received data. An important field of study is reducing data reception faults in wireless networks by changing the system design. The efficiency of such systems is better described by the receiver designs. In such a system, the Error Detection and Correction (EDAC) Decoder and Convolutional Encoder are incorporated in the transmitter and receiver, respectively. The wireless communication system's application of EDAC aids in cleansing the data of received mistakes. With the aid of the system design, a MIMO architecture based communication system offers a feature to decrease mistakes and enhance

channel bandwidth utilization. In order to provide large data capacity to the system users, communication designs choose a MIMO-based connection with EDAC.

The most widely used wireless communication standard in the industrial sector is IEEE 802.11. Researchers have put up a variety of changes that would enhance this communication standard's capacity for mistake detection and repair while maintaining the significance of other performance criteria. An FPGA-based MIMO-OFDM transceiver solution is shown in Reference [1]. The channel coder, its decoder, interleaver, and de-interleaver of MIMO-OFDM are explained in this reference FPGA implementation. Using MATLAB and an FPGA, the Wi-Fi wireless communication system is designed in reference [2]. The modeling and design of a wireless communication system based on the IEEE 802.11n draught are demonstrated in this study. VHDL is used to simulate the transmitter and receiver designs for FPGA-based implementation. References [3] through [4] provide a description of MIMO-OFDM implementation. A performance analysis of MIMO OFDM based wireless system is shown in the [5]-[8]. References [9]-[10] show a review on wireless communication system implementation. In the present work, the authors propose design of encoder, decoder, interleaver and de-interleaver for a MIMO-OFDM system. The design components are modeled using VHDL on Xilinx ISE Tool and the waveform based simulation analysis is performed on Xilinx ISim Tool. In this paper, section-II describes the Transmitter and Receiver sections of MIMO- OFDM based communication system. Section-III describes the proposed design blocks: Convolutional Encoder and Interleaver, Decoder and De-interleaver. Section-IV gives simulation results.

II. MIMO-OFDM SYSTEM ARCHITECTURE AND PROPOSED ENCODER-DECODER BLOCKS

Orthogonal Frequency Division Multiplexing (OFDM), a multi-carrier modulation technology, is widely utilized for data transmission and reception in wireless communication systems. Radio frequency carrier signals are used in the OFDM method for wireless signal transmission. The fundamental design of the MIMO-OFDM communication system is shown in Fig. 1. Such a system employs a convolutional encoder to encrypt the information-containing data.



It is usually preferable to use error detection and repair coding. The error-correction effectiveness of the decoder corresponding to the convolutional encoder has a direct relationship to the validity of the received data. Thus, this phase of the wireless communication systems is the most crucial phase. The complexity of the implementation circuit used to handle multiple-bit or burst errors place a restriction on the decoder's ability to detect and rectify errors. For addressing multiple bit mistakes, encoder/decoder and interleaver/de-interleaver circuits are typically employed. This reduces the complexity of the hardware. Consecutive bits or symbols are distributed in different packets or frames using an interleaver. By introducing a pause in the distribution of the subsequent data bits or symbols, this distribution protects the data from the effects of burst errors.

At the receiver end, the de-interleaver reorders the data into the correct sequence. The opposite action of De-Interleaver causes an even distribution of error among the data bits and symbols that are received. The Decoder block may then quickly process the de-interleaved data to find and fix the mistake.

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Fig.1. MIMO-OFDM Communication System Basic Architecture

Encoding using Viterbi Encoder with Interleaver:

The Viterbi Encoder & Interleaver makes the transmitter side of the proposed work. The 16-bit serially incoming bit is arranged in 8x8 matrix form first. This matrix form data is sent to the interleaver which changes the rows into column.

Let us explain the above process with the help of taking some example:

Consider the inputs for the Convolutional Encoder:

Input 16-bit – 1101001111001011

The encoded output of the Convolutional Encoder :

Encoder Output (Binary)-111 001011100 11101000 11101000 10010100 11000101 01111000 11001111

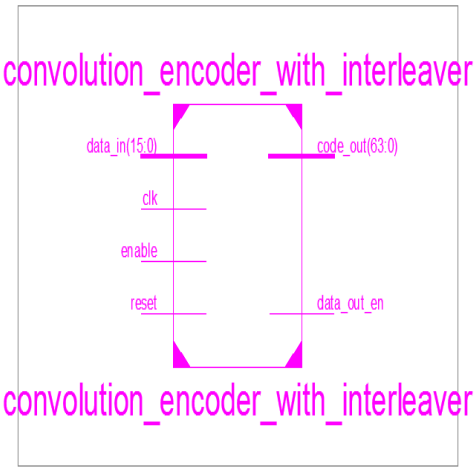
Now the inputs and outputs for interleaver will be:

Consider the inputs for the Interleaver:	The Outputs from the Interleaver are:
Input(64) bit – 11001111	Output(64) bit – 00000101
01111000	10000001
11000101	11001101
10010100	11110011
11101000	01001010
11101000	00110010
01011100	01110111
00001110	00111101

The output of the Convolutional Encoder with Interleaver :

Output 64-bit (Hexa)- 3d77324af3cd8105

This encoded output is arranged in matrix form before sending to the interleaver.



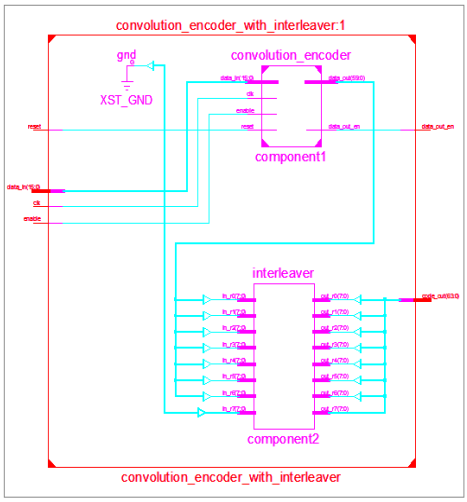


Fig.2. Block Diagram for Viterbi Encoder with Interleaver

Fig.3. RTL Schematic of Viterbi Encoder with Interleaver on

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Decoding using Viterbi Decoder & Deinterleaver:

In the receiver side of the communication system, we are using viterbi decoder and deinterleaver. The interleaver matrix form output is feded to the deinterleaver as input. The deinterleaver converts it into serial form and sent to the viterbi decoder. The viterbi decoder process the data and at the output of the viterbi decoder, 16-bit data is obtained which is same as transmitted from the transmitter , all burst errors are removed.

The above example is processed as follows:

Consider the inputs for the Deinterleaver :

Deinterleaver 64-bit Input - 00000101
10000001
11001101
11110011
01001010
00110010
01110111
00111101

The decoded output of the Decoder:

Decoder 16-bit Output (Binary) - 1101001111001011

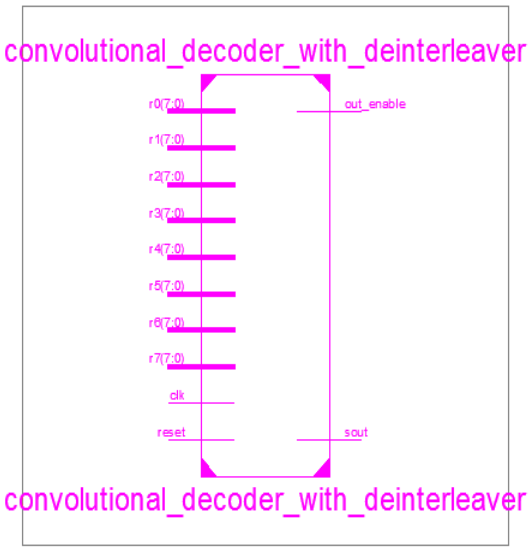

Fig.4. Block Diagram of Viterbi Decoder with Deinterleaver

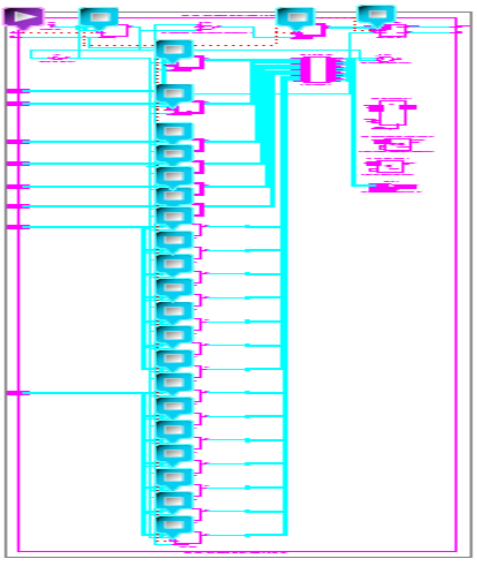

Fig.5. Block Diagram of Viterbi Decoder with Deinterleaver

III. RESULTS OF PROPOSED DESIGN SIMULATION

This work was created using the Xilinx ISE Tool and the VHDL language platform. VHDL Testbench on the Xilinx ISim Tool is used to simulate the design blocks. The waveform simulation results for the Viterbi encoder and Viterbi

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encoder with interleaver of the proposed work are shown in Figures 6 and 7. The suggested Viterbi decoder and deinterleaver waveform simulation results are shown in Figures 8 and 9.

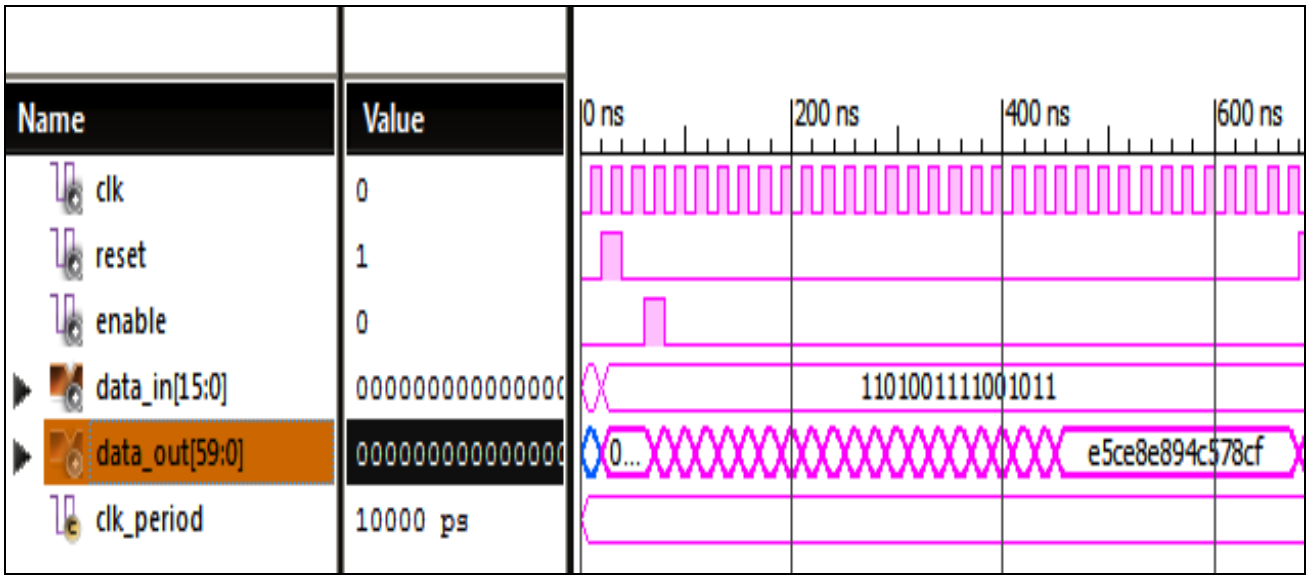

Fig.6. Simulation Waveform of Proposed Viterbi Encoder

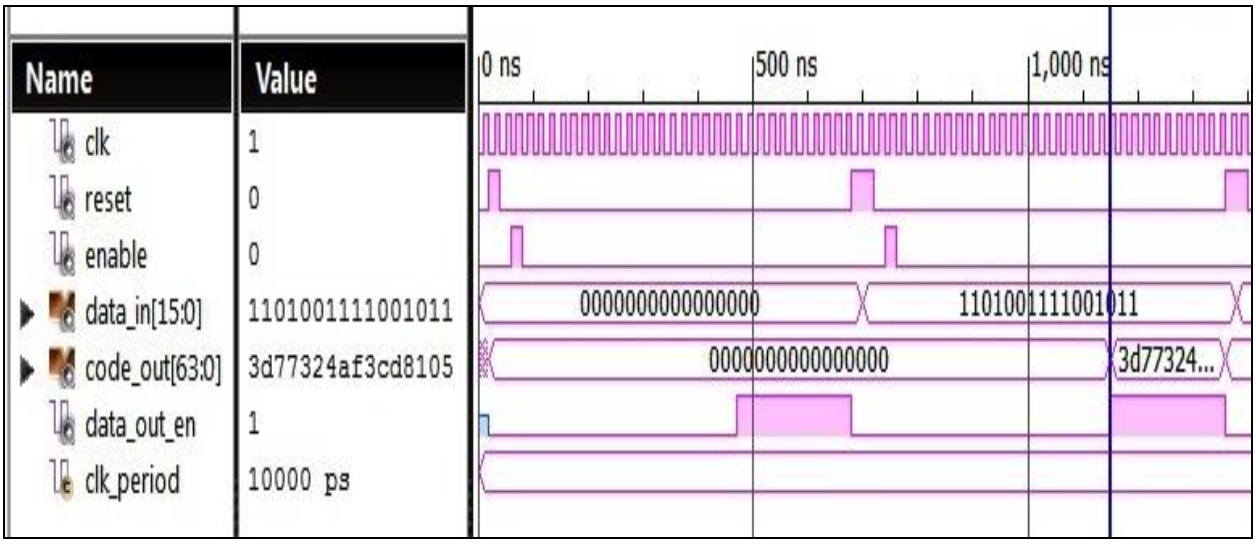

Fig.7. Simulation Waveform of Proposed Viterbi Encoder with Interleaver

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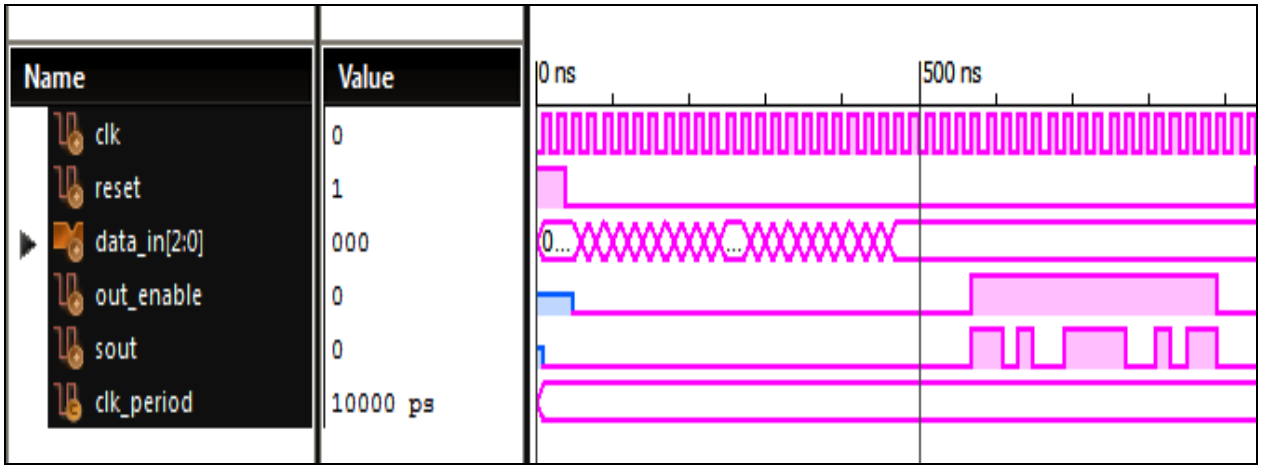
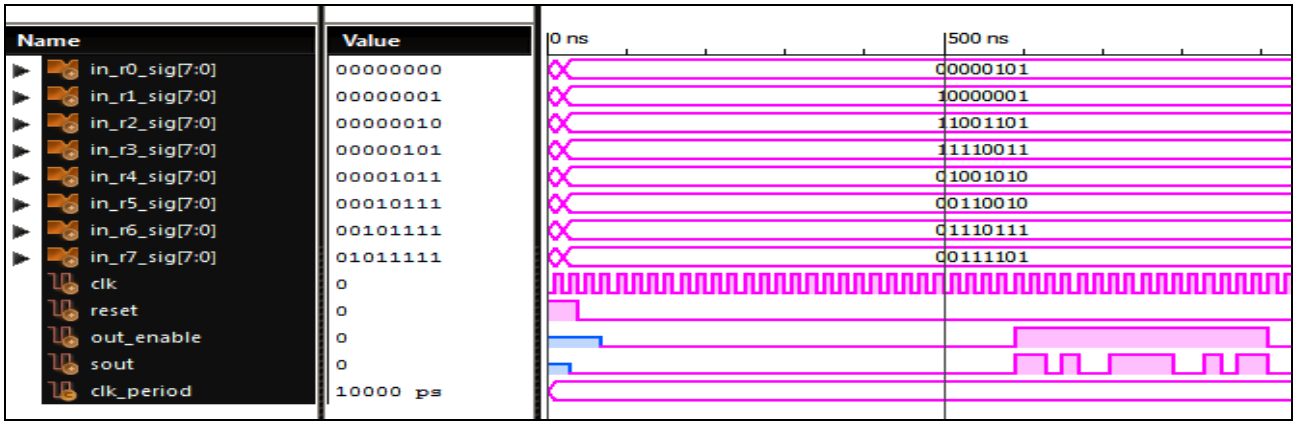


Fig.8.Simulation Waveform of Proposed Viterbi Decoder



Fi6 Fig.9.Simulation Waveform of Proposed Viterbi Decoder with Deinterleaver

The suggested solution is tested using communication hardware with burst error management capabilities. The suggested Encoder and Decoder architectures' FPGA-based hardware utilization summaries are shown in Tables, respectively.

Spartan-3E XC3S500E-4PQ208	Total	Encoder		Decoder	
		Used	%	Used	%
Slices	4658	151	3	437	9
Flipflops	9313	104	1	362	3
LUTs	9319	205	2	609	6

Spartan-3E XC3S500E-4PQ208	Reference Design		Proposed Design
	Input (4-Bit)	Input (4-Bit)	Input (16-Bit)
Device	Virtex-4 FPGA	Virtex-4 FPGA	*Spartan-3E FPGA*
Slices	195	780	158
Flipflops	104	408	103
LUTs	300	1200	201

IV. CONCLUSION

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A convolutional Decoder is a particularly efficient solution for identifying and fixing wireless communication faults. The amount of permitted complexity in the implementation method determines how many burst mistake bits a certain algorithm can correct using the Viterbi idea. Therefore, Interleaver is used in the proposed work to develop the EDAC method. A rate-1/3 An efficient approach for identifying and fixing single bit errors is the Viterbi Encoder. The suggested work displays a viterbi encoder/decoder design simulation for a wireless communication system based on MIMO-OFDM application. The suggested approach may be integrated successfully with typical communication apps to handle enormous amounts of data with a design that effectively identifies and corrects errors.

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