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" EFFICIENT WIRELESS DATA TRANSMISSION USING LOW COMPLEXITY TECHNIQUES"

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ABSTRACT

It's crucial to locate and fix any faults that may have occurred in the wireless communication route. One of the many error detection and correction (EDAC) algorithms that is often used is the Viterbi Decoder. Due to intrinsic drifting error between the estimated and correct path matrices and the optimal path matrices computation during the trellis generation, a high data-rate convolutional code experiences a drop in bit-error-rate performance. The availability of memory components, the circuit's decoding delay, the number of overhead bits in the algorithm, etc. are only a few of the numerous variables that greatly affect design performance. In this research, we present a design of a wireless communication system's Convolutional Viterbi Rate-1/3 Encoder and Decoder based on IEEE 802.11n Standard. The design and modelling of high data rate decoders is the main emphasis of the proposed effort. For functionality testing, the transmitter encoder and receiver decoder are built and simulated separately. The goal is to assess the viability of designing an Orthogonal Frequency Division Multiplexing (OFDM) multiple input multiple output (MIMO) wireless system data error detection and correction (EDAC) decoder. Because of its EDAC characteristic, the Viterbi Encoder/Decoder combo is highly useful in high data rate communication systems. Trellis coded modulation and de-modulation provide the foundation of the operational idea of viterbi encoding and decoding.

Key Words: *Trace back Decoder, convolutional viterbi rate, Xillinx, MIMO system , interleaver, OFDM.*

I. INTRODUCTION

In today's LAN-based systems, orthogonal frequency division multiplexing is successfully utilized for high data rate wireless communication. Establishing a data communication link between two nodes—the transmitter and the receiver—with no errors or as few errors as possible is the most crucial task in wireless networks. Using system architecture, the system provides a feature for reducing errors through MIMO-based communication. The system employs an error detection and correction-based technique to remove received errors introduced into the data by the wireless communication environment. Specialists have proposed numerous EDAC strategies with their efficiencies and execution highlights. Various factors, such as channel noise intensity, hardware speed, communication system type, and communication network type, are taken into consideration when selecting an effective EDAC implementation for a particular communication system. The College of Hawaii presented the main remote framework Salud net. Two wireless system standards were later developed: Both HIPERLAN and IEEE 802.11 However, HIPERLAN has not achieved commercial success. The authors have demonstrated the design of a wireless communication system in [1] to [2]. [3]-[4] provide an overview of the MIMO-OFDM implementation. The exhibition examination of MIMO OFDM based remote framework is displayed in [5]-[8]. The authors provide a summary of the implementation of the wireless

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communication system in [9]-[10]. The OFDM system's FPGA-based design is described in [11]–[14]. The convolution encoding and disentangling based Viterbi Decoder plan and execution is displayed in references [15]. In the proposed paper, segment II explains the Transmitter and Beneficiary areas of MIMO-OFDM based correspondence framework. The architectures of the convolutional Viterbi encoder and decoder are developed in Section III. The simulation results for the Encoder and Decoder designs are provided in Section IV. Section V provides a summary of the proposed work's conclusion and concludes with a mention of the references.

II. MIMO-OFDM ARCHITECTURE

Division of Orthogonal Frequency In wireless communication networks, multiplexing is a multi-carrier modulation technique that is widely used for data transmission and reception. Radio frequency carrier signals are utilized in OFDM to transmit wireless signals depicts a straightforward OFDM-based system. In such a system, the information-containing data is encoded using a convolutional coding approach, particularly one that includes error detection and correction. The most crucial component of such a system is this step. The effectiveness of the convolutional decoder's error correction directly relates to how well the data received match the information actually conveyed. The encoded data is subjected to data interleaving in the communication system. The encoded data is initially placed in a matrix during the interleaving process, and then the rows and columns are switched. By distributing errors uniformly throughout the received data stream, interleaving and de-interleaving aid in the recovery of data that has been damaged by burst errors. The data bits from the interleaved data stream are further grouped in the transmitter portion to correspond with the complex numbers denoting the kind of OFDM modulation. The kind of Quadrature Phase Shift Keying (QPSK) is then used to represent each mapped group of bits by a number that also indicates a certain sub-carrier phase and frequency

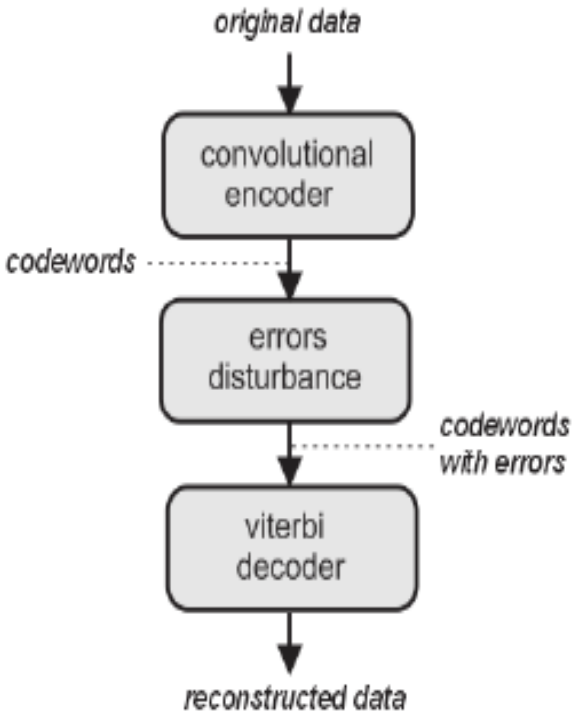

Figure 1 Block diagram of OFDM

III. CONVOLUTIONAL ENCODER:

A convolutional encoder is the viterbi encoder. Each serially received symbol is encoded with a predetermined number of output bit streams in the encoder. The rate of the encoder is determined by the amount of data bits in the input compared to the amount of data bits in the output. For each serially arriving bit, a rate=1/3 encoder produces three bits as encoded output, while a rate=3/4 encoder produces four bits as encoded output. The term "rate "p/q" encoder" refers to an encoder with 'p' number of input bits and 'q' number of matching encoded bits.

In the Encoder, the output logics S0, S1 and S2 are generated using the memory state and input logic and it can be represented using following equations:

S0 = S_inxor M2 xor M0 … (i)

S1 = S_inxor M3 xor M1 xor M0 … (ii)

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S2 = S_inxor M3 xor M2 xor M1 xor M0 … (iii)

Where, S_in is the serial input data bit, M0 M1, M2, M3 are states of the memory elements.

Consider the inputs for the Convolutional Encoder :
Input 16-bit – 1101001111001011
The encoded output of the Convolutional Encoder :
Encoder Output (Binary)-111 001011100 11101000 11101000 10010100 11000101 01111000 11001111
Encoder Output (Octel)- 713472164242461274317
Encoder Output (Hexa)-e5ce8e894c578cf

The output obtained from the Viterbi Decoder can be easily explained with the help of table shown in figure 2.

Figure Truth Table for Viterbi Encoder

	INPUT					OUTPUT			
CP	**S_in**	**M3**	**M2**	**M1**	**M0**	**S2**	**S1**	**S0**	**Octel Output**
↑									
	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	1	1	1	7
2	1	1	0	0	0	0	0	1	1
3	0	1	1	0	0	0	1	0	3
4	1	0	1	1	0	1	0	0	4
5	0	1	0	1	1	1	1	1	7
6	0	0	1	0	1	0	1	0	2
7	1	0	0	1	0	0	0	1	1
8	1	1	0	0	1	1	1	0	6
9	1	1	1	0	0	1	0	0	4
10	1	1	1	1	0	0	1	0	2
11	0	1	1	1	1	0	1	0	2
12	0	0	1	1	1	1	0	0	4
13	1	0	0	1	1	1	1	0	6
14	0	1	0	0	1	0	0	1	1
15	1	0	1	0	0	0	1	0	2
16	1	1	0	1	0	1	1	1	7
17	0	1	1	0	1	1	0	0	4
18	0	0	1	1	0	0	1	1	3
19	0	0	0	1	1	0	0	1	1
20	0	0	0	0	1	1	1	1	7

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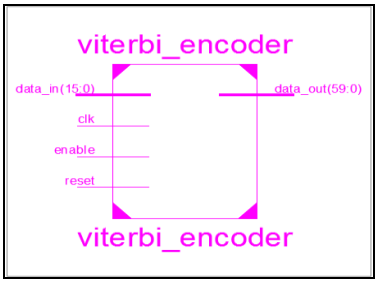

Figure 3 Block Diagram for Proposed Viterbi Encoder

IV. VITERBI DECODING

A Viterbi decoder unravels the convolutional encoder's bits-stream encoding. The decoder does this using the vitebi algorithm. There are several additional decoding methods for convolutionally encoded data streams, such as the Fano algorithm, but the Viterbi approach, which uses maximum likelihood, consumes the most resources. Convolutional codes with constraint lengths (K) between the values of (10–15) are often decoded using this method.A Viterbi decoder can be implemented in hardware (in modems) or software.

The error correction decoder, also known as the Viterbi Decoder, is a single bit error detection and correction decoder that is simulated in the current study. There is no burst error in the data since the decoder receives data from the De-Interleaver

Let us consider an example, which describes the process of Conventional Decoding:

The sequence which received is 11 01 01 10 01 which is error free and should be decoded.

The step by step procedure for decoding of given convolutionaly encoded data is given below.

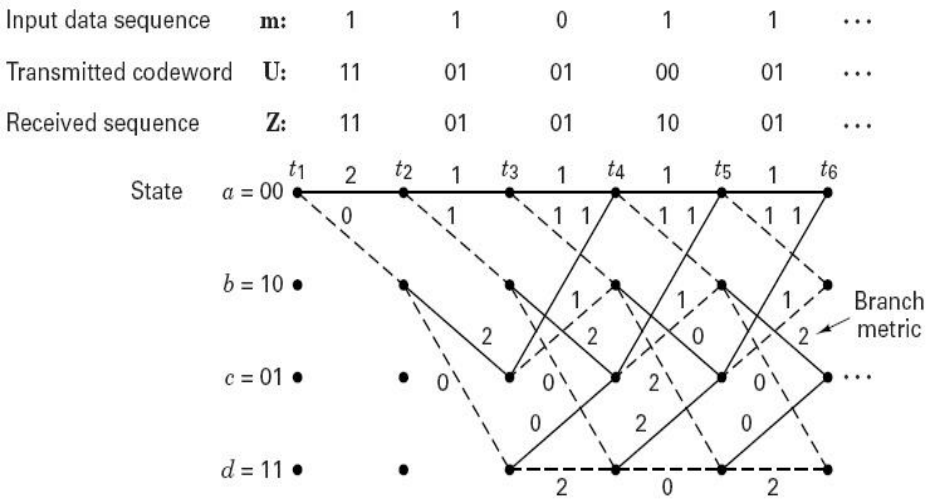

Figure 4 Trellis diagram for Convolutional Decoder

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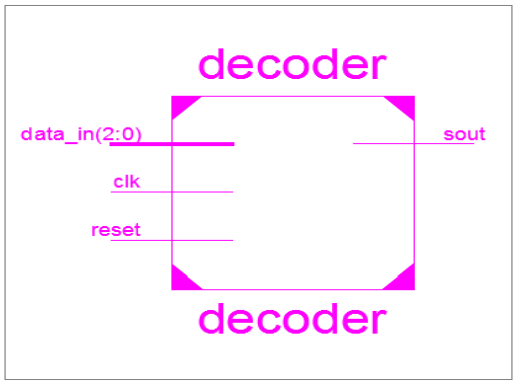

Figure 5 Trellis diagram for Convolutional Decode

V. INTERLEAVER

The suggested work's primary goal is to eliminate burst mistakes. Interleaver and deinterleaver circuits will make it simple to do this operation. The serially received data is initially organised in matrix form in the interleaver circuit. The rows are put in a column after interleaving.If there are faults in two consecutive bits, for example, the sequential burst defects are spread into single bit errors following the interleaving procedure. The viterbi decoder is a particular kind of decoder that can only be used to find and fix single-bit errors. Therefore, designers must spread burst faults into single ones. This work will be completed by the ease of Interleaver and deinterleaver circuits. The interleaver circuits will have little trouble completing this operation. At the transmitter end of the communication system, interleaver is employed.

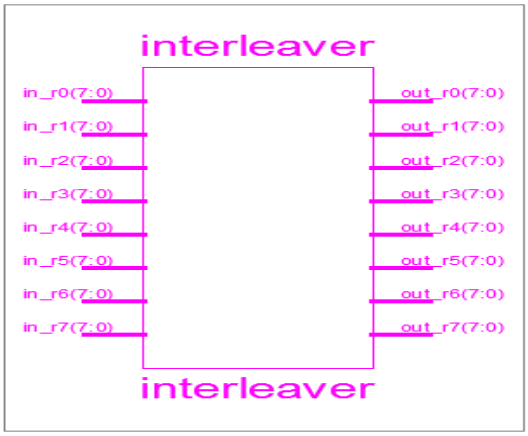

Figure 6 Block Diagram for Interleaver

VI. DEINTERLEAVER

Deinterleaver does the opposite task from that of interleaver. The receiver side of the communication system employs a deinterleaver. The deinterleaver receives input in matrix form, therefore it turns it into serial data that may be readily handled by the viterbi decoder in subsequent phases.

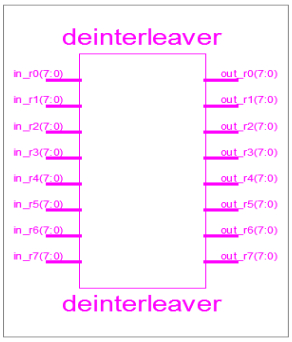

Figure 6 Block Diagram for Deinterleaver

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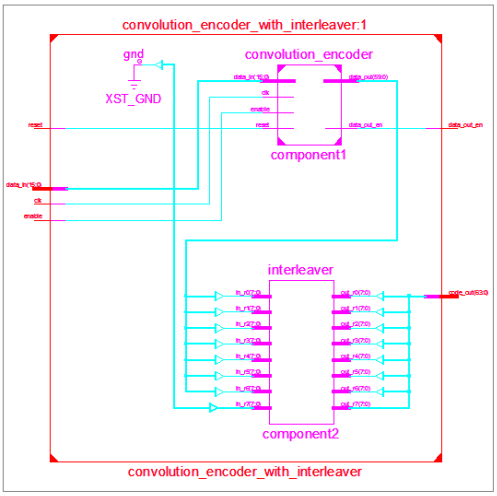

Figure 7 RTL Schematic of Proposed Viterbi Encoder with Interleaver on Xilinx

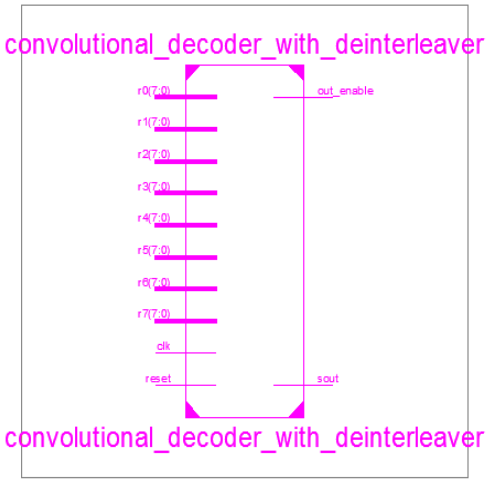

Figure 8 Block Diagram of Viterbi Decoder with Deinterleaver.

VII. SIMULATION RESULT

The inputs for the Convolutional Encoder:
Input 16-bit – 1101001111001011
The encoded output of the Convolutional Encoder :
Encoder Output (Binary)-1110010111001110100011101000100101001
100010101111000 11001111
Encoder Output (Octel)- 71347216424246127431 7
Encoder Output (Hexa)-e5ce8e894c578cf

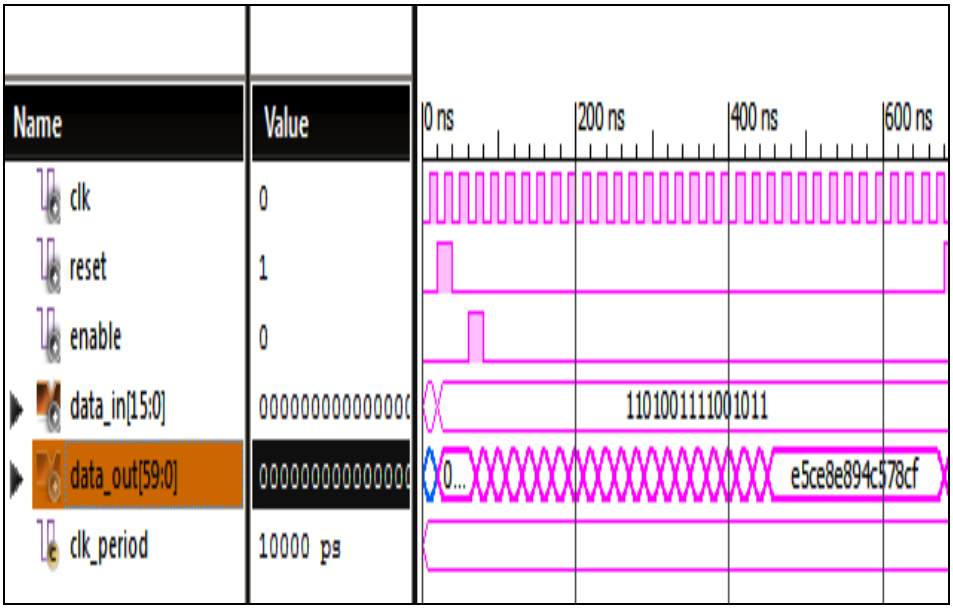

Figure 9 Simulation Waveform of Proposed Viterbi Encoder

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The decoded output of the Decoder :
Decoder 16-bit Output (Binary)- 1101001111001011

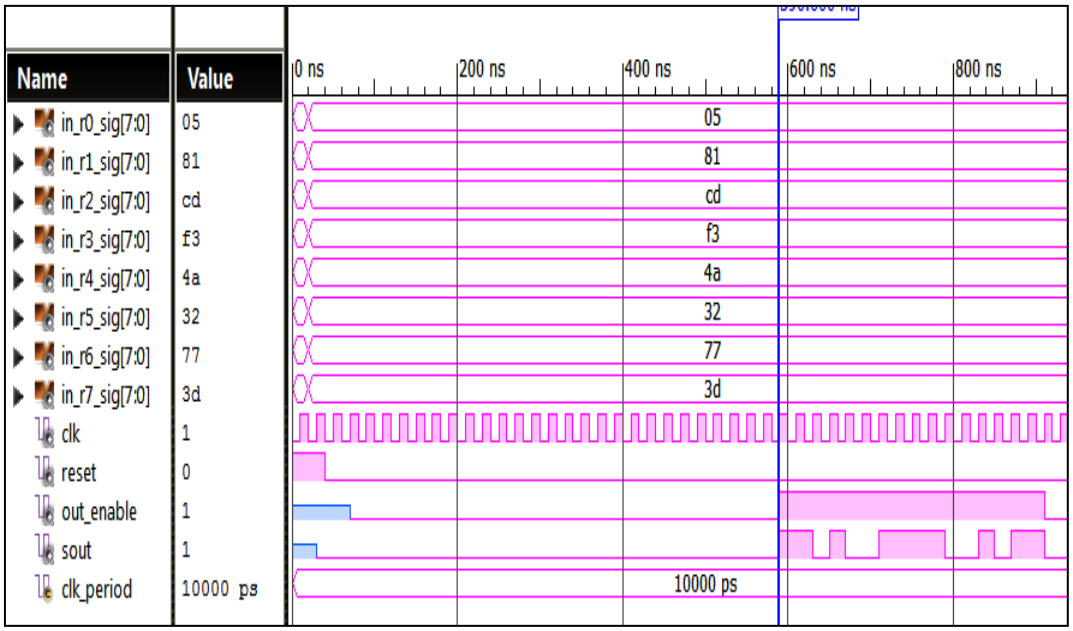

Figure 10 Proposed Decoder Simulation with NO error in received data

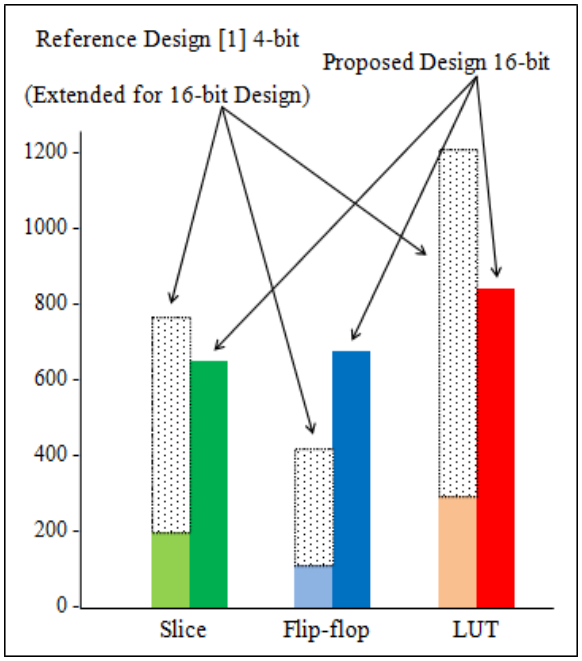

Figure 11 Comparison of H/w Requirement of Proposed Encoder/Decoder Design

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VIII. CONCLUSION

A Viterbi Decoder is an extremely efficient tool for identifying and fixing wireless communication issues. The maximum amount of error bits that may be rectified by a certain algorithm employing the Viterbi idea depends heavily on the implementation algorithm's permitted complexity. A rate-1/3 A single bit mistake in a transmitted symbol may

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be found and fixed with the help of the Viterbi Encoder algorithm.

Example-2: simulation with error in transmitted data and error-correction by decoder

Input 16-bit 1011011001101101

Encoder Output (Binary) 111 110 010 111 100 100 0**1**0 100 011 110 **00**0 011 100 000 100 100 111 010 11**1** 111

Encoder Output (Octal) 76274404366340447267

Encoder and Decoder simulation waveforms are shown inFig-9 and Fig-10 respectively.

The proposed work displays a design simulation of a multiple-input multiple-output (MIMO) OFDM-based rate-1/3 viterbi encoder and decoder. The suggested approach may be applied to large-scale data successfully while preserving the design's capacity to detect and repair errors.

REFERENCES

[1] AshishTripathi, Anil Kumar, A.K. Jaiswal, Rajeev Paulus and Mayur Kumar, "Low complexity data transmission over wireless system", International Journalof Current Engineering and Technology (IJCET), Volume-4 Issue-3 June 2014..
[2] Allan Lopes and ZahirAalam, "Performance Analysis of 802-11n OFDM Transceiver", International Journal of Engineering Research and Applications, Volume-4 Issue-7, July 2014.
[3] Mr. BhavinGamit and Prof. Shweta N. Shah, "Performance Analysis of 2x2 MIMO for OFDM-DSSS based Wireless System", International Journal of Innovative Research in Advanced Engineering (IJIRAE),Volume-1 Issue-5 June 2014.
[4] Alisha Khan and SourabhShrivastava, "Performance Evaluation of OFDM System for Bluetooth Fixed and Mobile Wimax Application", International Journal of Advance Research and Innovation, Volume-2 Issue-2,2014 .
[5] MadhusudanKar, SwarnalataPatra, Kundan Kumar, Chinmayee Das and Priyanka Nanda, "Relative Analysis of Transceiver Diversity and Channel Estimation of MIMO OFDM", International Journal of Advanced Research in Science, Engineering and Technology,Volume-2 Issue-1, January 2015.
[6] Saran M. L., T. C. Manjunath and HarshaKaramchandani, "Simulation of Comm channels using FPGA/VHDL - A brief review with implementation concepts using hardware and software", International Journal of Electronics and Communication Engineering, Volume-2 Issue-5, May 2015.
[7] AmitSaini and VijayaBhandari, "OFDM Transmission and Reception: Review", International Research Journal of Engineering and Technology, Volume-2 Issue-2, May 2015
[8] K. Srinandhini and V.Vaithianathan, "FPGAImplementation of MIMO-OFDM Transceiver", International Conference on Communication and Signal Processing, April 2014.
[9] Gaurav S Bhangle, "VLSI Design in MIMO OFDM for Wireless LAN Networks", International Journal of Engineering Research and Applications (IJERA),Volume-3 Issue-4, 2013.
[10] E. Konguvel, J. Raja and M. Kannan, "A Low Power VLSI Implementation of 2x2 MIMO OFDM Transceiver with ICI-SC Scheme", International Journal of ComputerApplications (IJCA), Volume-77 Issue-5, September 2013.
[11] Pratibha Mane, VarshaThombare, MonaliMhaske and R. R. Bhambare, "Implementation of 802.11n OFDM Transmitter and Receiver using FPGA", International Journal of Engineering Technology and Advanced Engineering, Volume-4 Issue-4, April 2014.
[12] Arjit Mukherjee, "Viterbi Decoding for OFDM systems operating in narrow band interference", Thesis submitted at Waterloo Ontario Canada, 2009.
[13] MahendraBabu D. S., Vinutha M. R. and Uma C., "Design and Implementation of MIMO-OFDM using Encoding and Decoding techniques on FPGA", International Journal of Scientific and Engineering Research, Volume-5 Issue-6, June 2014.
[14] K. S. Arunlal and S. A. Hariprasad, "An Efficient Viterbi Decoder", International Journal of Advanced Information Technology (IJAIT), Volume-2 Issue-1, February 2012.
[15] http://www.mathworks.com/examples/phased- array/4581-beamforming-for-mimo-communication-systems..