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# "OPTIMIZED CONVOLUTIONAL DECODER WITH RATE-1/3 FOR MIMO-OFDM SYSTEM: DESIGN AND SIMULATION"

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## ABSTRACT

***The Viterbi Decoder's architecture and modeling for a wireless communication system with multiple inputs and multiple outputs are presented in this study. Identifying errors introduced into wireless environment signals is essential for confirming the receipt of reliable data. Transmitters and receivers are constantly exchanging massive volumes of data as a result of improvements in wireless communication technology. This data is affected by several other communication signals, noise created randomly by machines, noise made by people, and noise made by nature. To generate the original sent data, the receiver requires a suitable method. A system like this ensures precise data processing and stops the production of any unwanted output. By creating an error detection and repair Viterbi decoding method, the current work successfully corrects a single bit error that occurred during the transmission of an encoded data signal. Software from Xilinx is utilized to validate the simulation.***

***Key Words:*** *Multiple Input Multiple Output, Orthogonal Frequency Division Multiplexing, Wireless communication system, Viterbi decoder, Xilinx.*

## I. INTRODUCTION

Data integrity is a very important feature of all the communication receiver hardware. This feature would be designed with multiple input multiple output OFDM system. A convolutional encoding hardware would be realized for such a communication system. And an interleaver circuit would also be synthesized for the system. The concept of interleaver and de-interleaver helps to evenly distribute the received errors among the received data bits. This makes the receiver hardware to analyze the errors in distributed parts and hence making the availability of less complex error handling hardware more effective against some burst errors also. In such a system, the transmitter and receiver each have a Convolutional Encoder and its associated Error Detection and Correction (EDAC) Decoder. The use of EDAC in a wireless communication system aids in the removal of received mistakes from data. With the aid of system architecture, a MIMO architecture-based communication system provides a feature to decrease mistakes and enhance channel bandwidth utilisation. As a result, communication designs favour MIMO-based communication with EDAC to provide large data capacity to system users.Error detection encoding schemes detect the errors introduced in the environment. These techniques are helpful for any type of errors whether error is introduced in single bit or the errors are introduced in more than one bit ie (burst error ).Error correction encoding scheme correct the errors which are detected by the error detection encoding scheme. It can correct error more than one bit. These techniques reconstruct the original signal and make the signal which is free from errors.

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## II. VITERBI ENCODING & DECODING

It is the most popular error detecting and correcting encoding scheme. This scheme is generally suited with the convolutional encoder. Viterbi decoding with convolutional encoding makes the communication system which is very robust against noise which is introduced in the wireless environment. This system is a good forward error correction technique and best suited for the channels which are affected by noise degradation.

Convolution coding is a very popular error-correcting and detecting coding technique used in modern wireless communications system. In this encoding method, a message signal is encoded with additional number of bits at the transmitter side, and then transmitted into a noisy channel environment. The noise which are introduced in the environment is remove at the receiver side with the help of viterbi decoder.

The Viterbi algorithm is a popular algorithm used to decode convolutionally coded messages signal.The algorithm follows the most likely state sequences of data and went through in encoding by using this information to find out the original message signal. The convolutional encoding and Viterbi decoding process the data in package form and encodes a message as a sequence of data.

**2.1.1 Convolutional Encoder**:

A convolutional encoder is generally represented by ( n,k,m) where (n) is the number of encoded bits, (k) is the total number of bits at its input or the bits which is going to be encoded and (m) is the memory length of the register. Convolutional codes are commonly described using two parameters ie Code rate and the Constraint length. The code rate of the enocoder is generally represented by:

**Code Rate = k/n**

which is the ratio of number of bits at the input of the encoder and the number of bits at its output.
The constraint length parameter (K), denotes the "length" of the convolutional encoder It tells the number of states required for the encoder for producing its final output .The constraint length of the encoder is generally find out by the help of formula as shown below:

**Constraint Length (K) = k (m-1)**

Suppose we have a convolutional encoder of (3,1,4) in which for every single bit the encoder produces the data of 3 bit with the help of 4 memory element ie flip flops. The code rate for this type of encoder is:

**Code rate = 1/3**

**&**

**Constraint Length (K) = 1(4-1) = 3 (23 = 8 )**

This means that the encoder requires minimum (8) number of possible states for producing its final output.

Convolutional codes are widely used in practical communication systems as channel codes for error correction. The encoded bits depend on the few past input bits and current (k) input bits. The decoding process for convolutional codes is generally done by Viterbi algorithm. In this diagram of convolutional encoder, two flip flops are used ie shift register, generally we are using D flip flops here and two XOR gates are used.

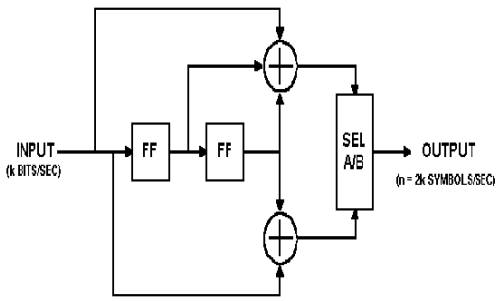


**Figure 1.Block Diagram for Convolutional Encoder**

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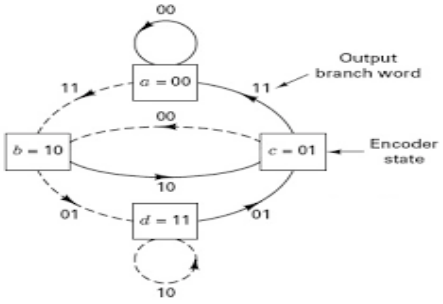


**Figure 2.State Diagram**

| Input | Present State | Next State | Output |
|---|---|---|---|
| 0 | 00 | 00 | 00 |
| 1 | 00 | 10 | 11 |
| 0 | 10 | 01 | 10 |
| 1 | 10 | 11 | 01 |
| 0 | 01 | 00 | 11 |
| 1 | 01 | 10 | 00 |
| 0 | 11 | 01 | 01 |
| 1 | 11 | 11 | 10 |

**Table 3. State Table**

### 2.1.2 Trellis Diagram of Convolutional code:

The trellis diagram of a convolutional code is generally drawn from its state diagram. For every state, there are two possible conditions to move further and we can determine it with the help of state diagram, next states are defined by for every '0' and '1' of possible input of state.

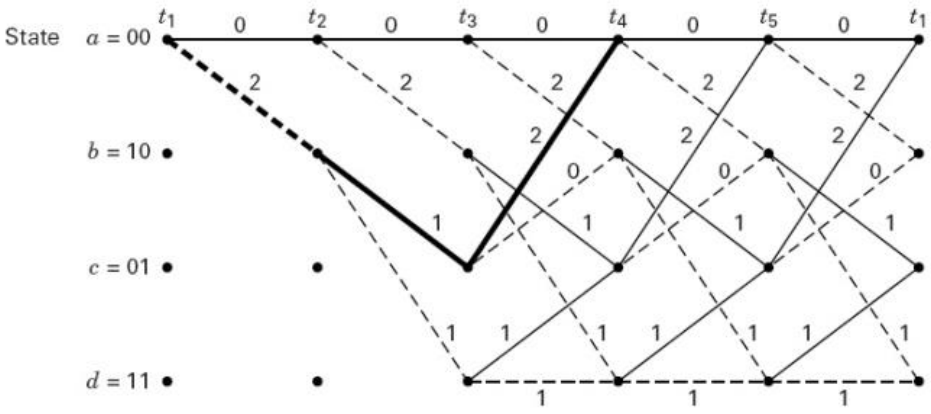


**Figure 4.Trellis diagram for Convolutional Encoder**

### 2.2 Encoder in Proposed work:

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A convolutional encoder is the viterbi encoder. Each serially received symbol is encoded with a predetermined number of output bit streams in the encoder. The rate of the encoder is determined by the amount of data bits in the input compared to the amount of data bits in the output. For each serially arriving bit, a rate=1/3 encoder produces three bits as encoded output, and a rate=3/4 encoder produces four bits as encoded output. The term "rate "p/q" encoder" refers to an encoder with 'p' number of input bits and 'q' number of matching encoded bits.

Current input data and the state of the encoder register are combined to create the encoder output. All of the encoder registers and the encoded output bits will be driven to the logic "0" state by a continuous sequence of up to four input "0" bits. The encoder is also in this initial form at this point. The minimal '0'-bit at the input necessary to reset the encoder depends on how the encoder registers are currently configured. The number of flip-flops or memory cells employed in the encoder serial shift-register determines the encoder's length. In the current work, a rate=1/3 viterbi encoder with four flip-flops in the encoder shift-register is simulated. Fig. 5 depicts the production of the output logic.

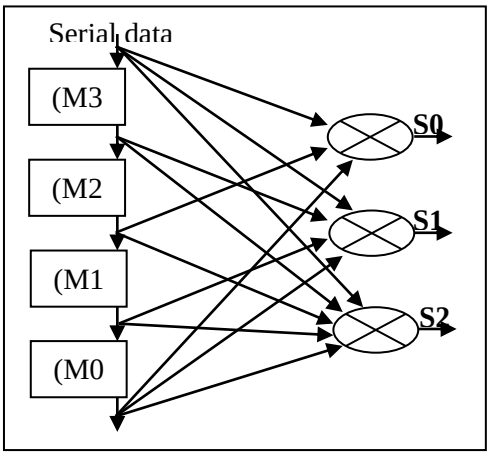


**Figure 5. Viterbi Encoder output logic**

input logic and it can be represented using following equations:

S2 = S_inxor M3 xor M2 xor M1 xor M0 … (i)
S1 = S_inxor M3 xor M1 xor M0 … (ii)
S0 = S_inxor M2 xor M0 …… (iii)

Where, S_in is the serial input data bit, M0 M1, M2, M3 are states of the memory elements.

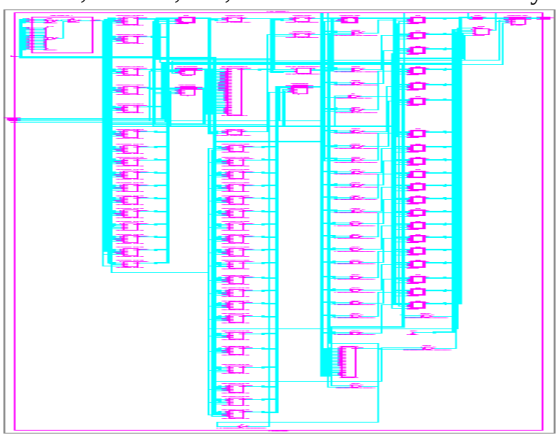

**Figure 6. RTL Schematic of Proposed Encoder on Xilinx**

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### 2.3 Viterbi Decoding:

A Viterbi decoder decodes the bits stream which is encoded by the convolutional encoder. The decoder uses the vitebi algorithm for this purpose. There are many other algorithms for decoding a convolutionally encoded data stream but Viterbi algorithm is the most resource-consuming. It is generally used for decoding of convolutional codes with constraint lengths (K) between the value of (10-15).There are both software and hardware (in modems) implementations of a Viterbi decoder.

The Error correction decoder, i.e., Viterbi Decoder that is simulated in the present work is a single bit error detection and correction decoder. Since the decoder is provided data from the De-Interleaver, no burst error is present in the data. So, the decoder can easily correct the distributed errors using its single bit error correction ability.

The Viterbi Decoder operation is based on the calculation of bit changes in every step of the decoding process. The decoder receives encoded symbol serially. On the basis of bit change in the estimated data, the decoder calculates *State-Metric*, *Path-Metric* and *Branch-Metric* for computing the best estimated value of the transmitted bit. The estimated data is retrieved by back-trace processing of data bits from the path of the *Branch-Metric*, i.e., the path that shows minimum bit change during decoding.

Using a flow diagram, the viterbi decoder's decoding steps are displayed in Fig.7. Branch and path metrics are computed using the serially received data. Based on the difference between the number of bits in the received data bits and the anticipated bits, the metric computation is performed. By back-tracing the data bits on the path with the lowest path metric value—i.e., the path with the fewest bit changes during decoding—the estimated data is taken into account.

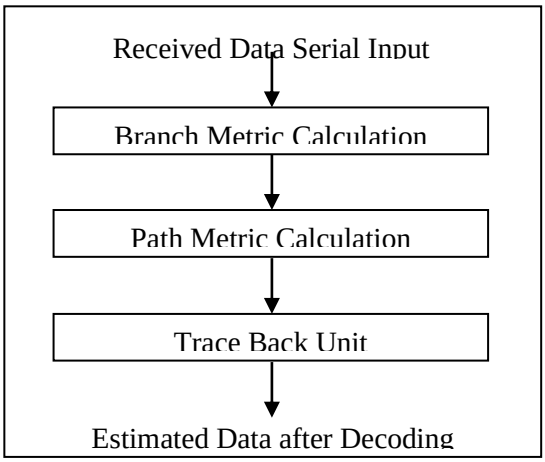


**Figure 7. Flow Chart for Viterbi**

Let us consider an example, which describes the process of Conventional Decoding:

The sequence which received is 11 01 01 10 01 which is error free and should be decoded.

The step by step procedure for decoding of given convolutionaly encoded data is given below.

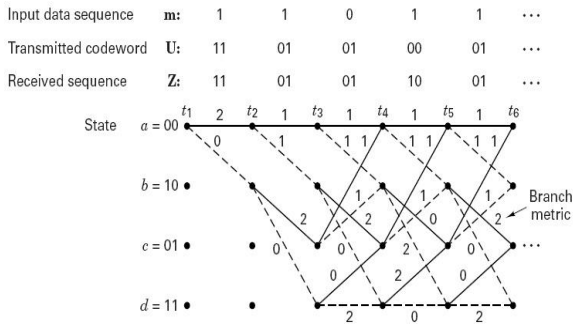


**Figure 8. Trellis diagram for Convolutional Decoder**

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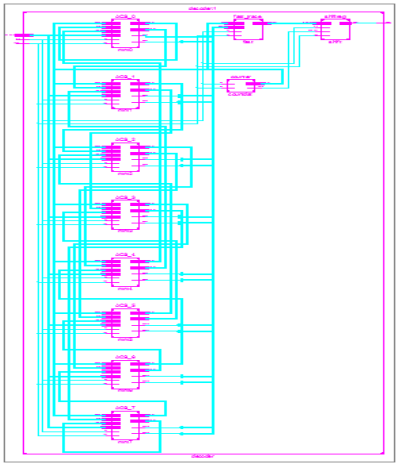

**Figure 9. RTL Schematic of Proposed Decoder on Xilinx**

## III. PROPOSED DESIGN SIMULATION:

This work is designed on VHDL language platform on Xilinx ISE Tool. The simulation of the design blocks is performed using VHDL Testbench on Xilinx ISim Tool. Fig.10 and Fig. 11 represent the waveform simulation result of the decoder with 16 bit error and no error received.

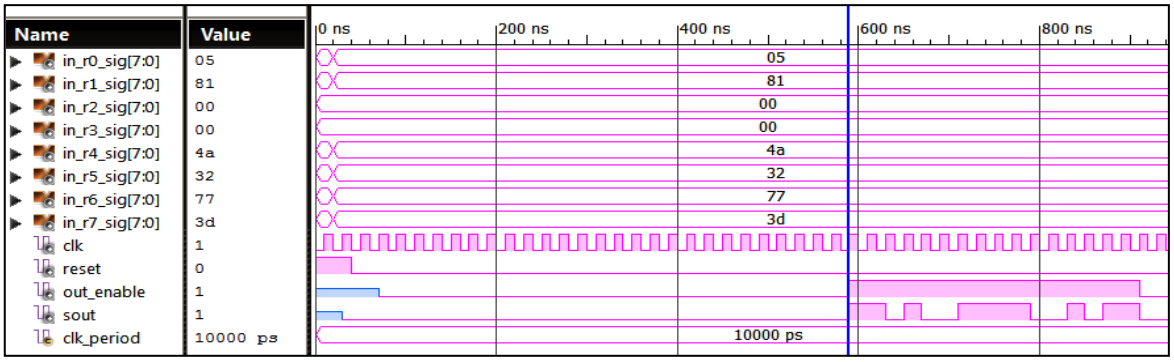


**Figure 10**

## IV. CONCLUSION

Orthogonal frequency division multiplexing (OFDM) and multiple input multiple output (MIMO) technology have recently received a lot of attention. Through spatial multiplexing, MIMO delivers excellent spectral efficiency, whereas OFDM gives robustness against interference brought on by multipath propagation. With a focus on transceiver design, this article offers a high-level study of the fundamentals of MIMO-OFDM wireless systems. According to a literature review, MIMO-OFDM has significantly improved and is now the best option for 4G networks, home entertainment networks, and wireless LANs.

## V. FUTURE WORK:

Future improvement scope is always a part of any proposed design work. In the proposed work there would be a scope of re-structured architecture of the encoding hardware design for the new emerging technologies and the future hardware requirements. An improvement in the error handling efficiency of the proposed work can also be an

additional advantage that can be selected by researchers in the future to work on.

The suggested work displays a viterbi encoder/decoder design simulation for a wireless communication system based on MIMO-OFDM application. The suggested approach can be introduced successfully with typical communication apps to handle enormous amounts of data with a design that effectively identifies and corrects errors. The proposed work shows a MIMO-OFDM application based design simulation of viterbi encoder/decoder for a wireless communication system. The proposed concept can be introduced effectively with common communication applications to handle large sized data with an effective error identification and correction ability of the design.

In future, the proposed work can be implemented in mobile applications for inter-mobile data transfer using mobile applications. The proposed work can be improved in future by implementing it with other existing EDAC algorithms for an improved efficiency Xilinx ISE Design Tool for VHDL design entry and Xilinx ISIM for hardware performance simulation for functional verification will be used to design and model the proposed work. For various Xilinx Field Programmable Gate

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